Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 – 14. (canceled)

15. (currently amended) A memory device comprising:

an interface for receiving access requests, the interface having an address output to an address path and a data output to a data path, wherein address information is carried on the address path and data for writing to memory or data read from memory is carried on the data path;

a memory cell array having a plurality of low-latency, rewritable, non-volatile memory cells forming at least one memory section;

a word-select unit connected in the data path and to the address path and between the interface and the memory cell array to provide column selection;

a section-select unit connected to the address path and between the interface and the memory cell array to provide row selection;

wherein both the word-select unit and the section-select unit select a respective column and row of the memory cell array in response to the address information;

a profile storage unit connected to said interface comprising a plurality of request profiles that each represent a profile of an access request, wherein each request profile includes:

a set of request information elements, wherein at least one of the request information elements indicates whether an access request is a read request or a write request; and

an access flag whose state indicates whether a corresponding access request is allowed to access the memory or not allowed to access the memory;

an access control unit connected to said profile storage unit and said memory and configured to allow or reject an access request;

wherein said profile storage unit selects an access flag that corresponds to a request profile in response to an access request that fits the request profile; and

wherein the access control unit allows or rejects an access request in response to the access flag that is selected by the profile storage unit.

16. (previously presented) The memory device of claim 15 wherein the profile storage unit comprises a set of access flags, one access flag for each row address, such that each access flag governs the access to one row of the memory cell array.

17. (previously presented) The memory device of claim 16 wherein the access flags are fast read-out state registers.

18. (currently amended) The memory device of claim 15 wherein the access control unit operates in the ~~a~~ data path to admit or reject a flow of data to or from the memory cell array depending on the state of the corresponding access flag it receives from the profile storage unit.

19. (previously presented) The memory device of claim 15 further comprising a memory mapped interface and an I/O mapped interface connected to provide access to the memory cell array.

20. (previously presented) The memory device of claim 19 wherein pins of the memory device are shared by the memory mapped and I/O mapped interfaces.